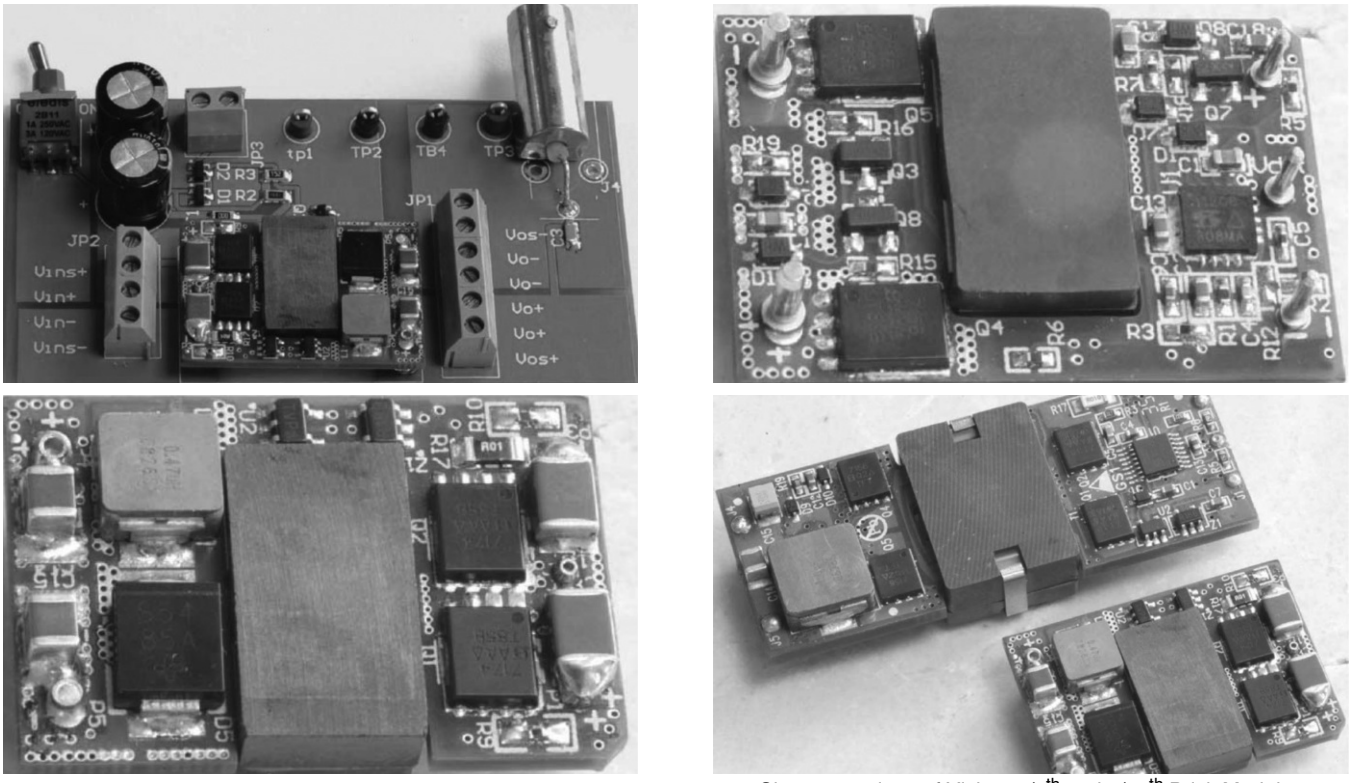
200 W 1/16th Brick IBC Demo Board using SiP11206

DESCRIPTION

SiP11206 is a half-bridge controller for intermediate bus converters. While SiP11206 allows for overall better efficiency through out the input voltage range, since its duty cycle is fixed and is optimally set closer to its maximum 50 %. This also limits the input voltage range to a narrower 42 V to 55 V typical range because of the fixed duty cycle the output voltage will have a proportionally wider voltage swing. The SiP11206 is best for applications where efficiency is key and a wider output voltage can be tolerated. This demo board is a sixteenth-brick IBC power converter, which plugs into a baseboard. The IBC board has the following specifications and options:

- Narrow input voltage range (42 V to 55 V) with SiP11206 controller IC
- Nominal 12 V output, nominal load current 17 A
- PowerPAK® 1212-8 for primary and secondary power MOSFETs

The baseboard contains input fuse, input/output terminals, remote enable connectors, enable switch, input bulk capacitors and output voltage measurement BNC connector. The cutout in the baseboard allows for probing of both sides of the IBC board. Photos are shown in figure 1.



Size comparison of Vishay 1/8th and 1/16th Brick Modules

Figure 1. Photos of Demo Board with PowerPAK MOSFET Options

This document details the following of the demo board:
1. Set up
2. Operation
3. Waveforms and performance curves
4. Schematic and BOM
5. Board layout

SET UP

The connection diagram for the demo board is depicted in figure 2. Power and sense connections are provided at the input and output for the main current path and for voltage sensing for efficiency monitoring. Wire rated at 5 A should be used for the input connections and 2 x 10 A rated wire should be used for the output lines. The board can be enabled/disabled manually by using the on-board switch or by connecting a 0 V/5 V logic signal in the disable connector. 5 V represents ‘disable’.

Wiring lengths should be kept as short as possible, especially at the output in order to avoid excessive voltage drop across the cable length. The demo board has two 47 µF capacitors at the input to help minimize the issues with long cables lengths used at the input. It should be noted that with long cable lengths, the input voltage might be quite oscillatory on power up, potentially leading to under-voltage or the converter cycling in and out of operation until the voltage becomes steady.
A small fan should be placed so that air is blown over both sides of demo board in the direction shown. If the temperature of the board exceeds ~ 105 °C, the board will be disabled by the over temperature shutdown mechanism.

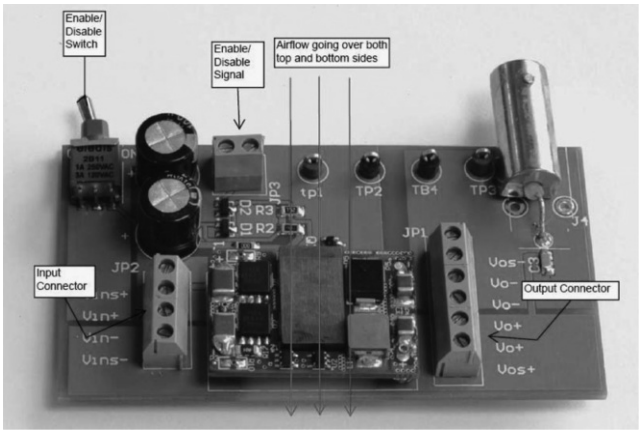
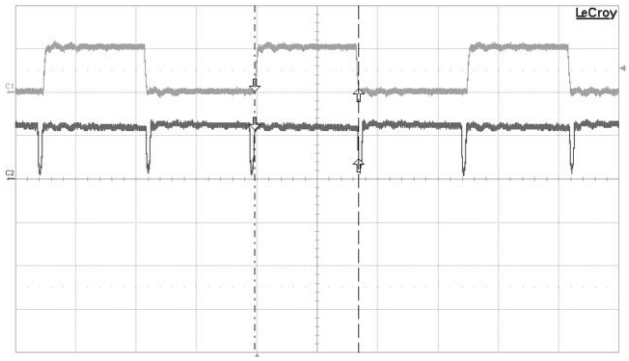


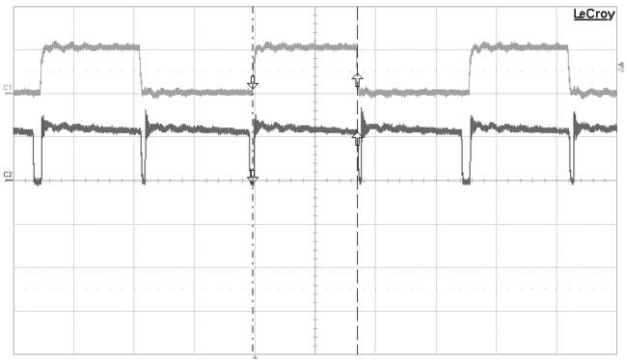
Figure 2. Connection Diagram

OPERATION AND TEST RESULTS

The power circuit is a half-bridge converter controlled by the SiP11206 IC. In the SiP11206, the converter duty cycle is fixed and is set by R_2. This version of the chip was used on the demo board which maintains the highest overall efficiency since the duty cycle is constant. It is typically set to a value close to 50 % for maximum efficiency. The output voltage is then determined by the input voltage and the transformer turns ratio. In this demo board, the transformer turns ratio is 4:1.
The controller IC is powered at startup by its own internal 9.5 V pre-regulator, which is driven from the line voltage. Once converter switching commences, a separate 10.3 V V_{CC} supply is supplied from an auxiliary transformer winding, and linear regulator R_{18}, Q_7, D_8.
The secondary side synchronous rectifiers are self-driven, but with a controlled gate voltage that does not vary with input voltage. The result is improved efficiency and safer drive voltages because the secondary gate drive is generated locally and clamped to ~ 10 V through D_9, R_{19}, C_{12} and D_{10}. MOSFETs Q_8 and Q_3 are triggered by the opposite transformer node, and the 10 V is coupled to the synchronous rectifier gate less a threshold voltage drop.
A Schottky diode can be connected across the output filter which improves efficiency for longer dead times. During dead time, the synchronous rectifiers are off as there is no transformer voltage available to turn them on. Hence, without the Schottky diode present, the inductor current will flow through the body diodes of the synchronous rectifiers. The Schottky diode has a smaller voltage drop than the body diodes, and so may enhance efficiency dependent on deadtime, sync-fets, layout etc…. Some typical converter waveforms are shown in figures 3 to 7.

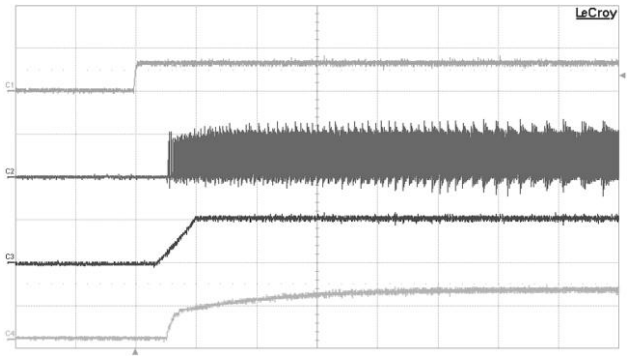


(a) 48 V with 0 A, 1 DL, 2 V_{LOUT}

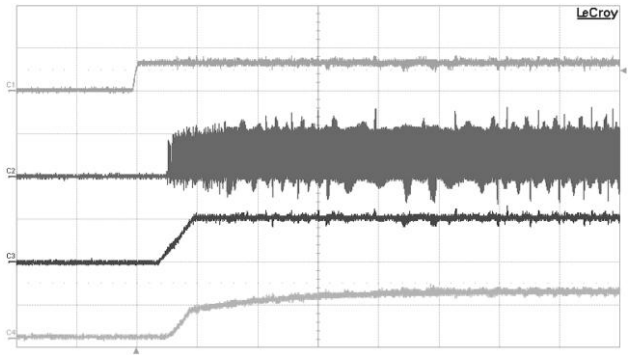


(b) 48 V with 10 A, 1 DL, 2 V_{LOUT}

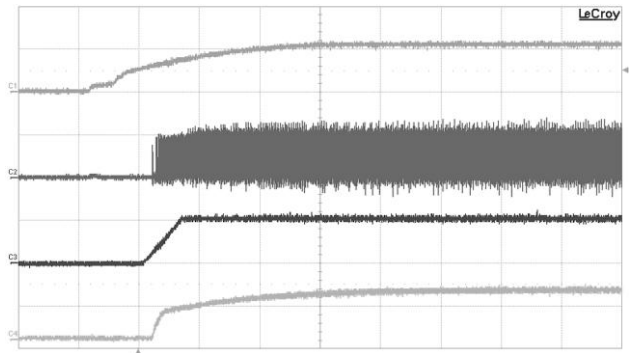
Figure 3. Secondary Switching Waveforms



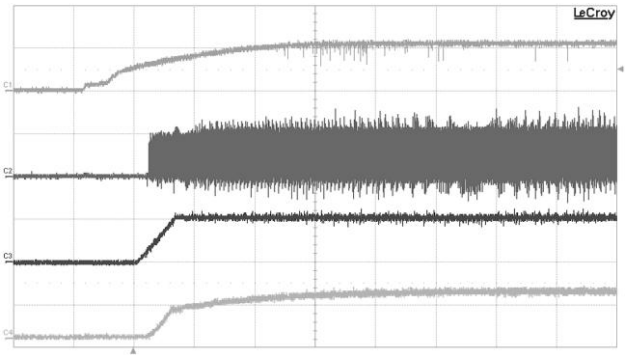
Startup 0 A Load 1 V_{REF}, 2 DL, 3 SS, 4 V_{OUT}



Startup 10 A Load 1 V_{REF}, 2 DL, 3 SS, 4 V_{OUT}

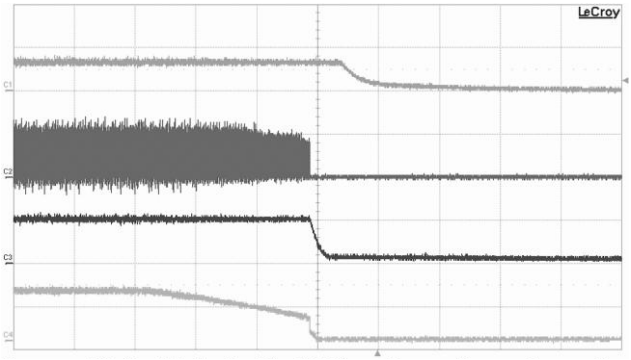


Startup 0 A Load 1 V_{DET}, 2 DL, 3 SS, 4 V_{OUT}

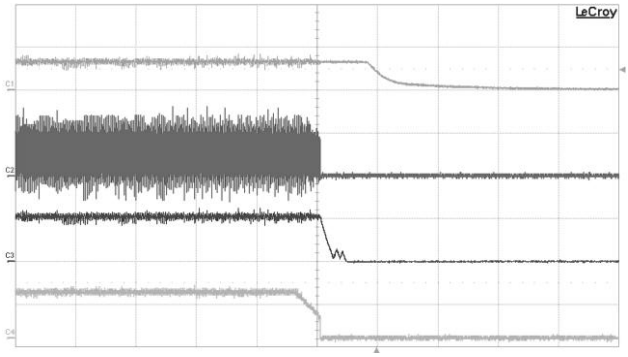


Startup 10 A Load 1 V_{DET}, 2 DL, 3 SS, 4 V_{OUT}

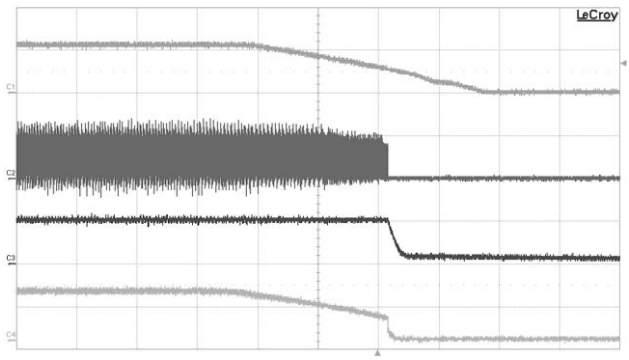
Figure 4. Startup Waveforms



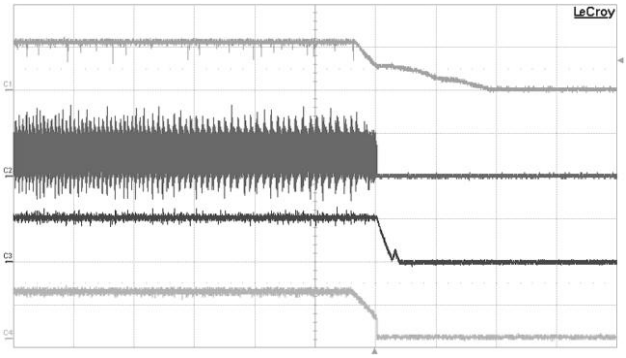
Shutdown 0 A Load 1 V_{REF}, 2 DL, 3 SS, 4 V_{OUT}



Shutdown 10 A Load 1 V_{REF}, 2 DL, 3 SS, 4 V_{OUT}

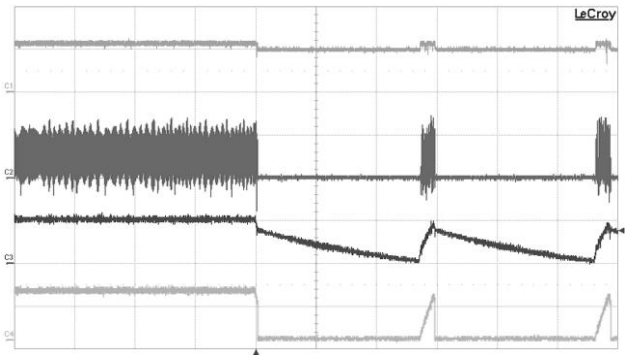


Shutdown 0 A Load 1 V_{DET}, 2 DL, 3 SS, 4 V_{OUT}

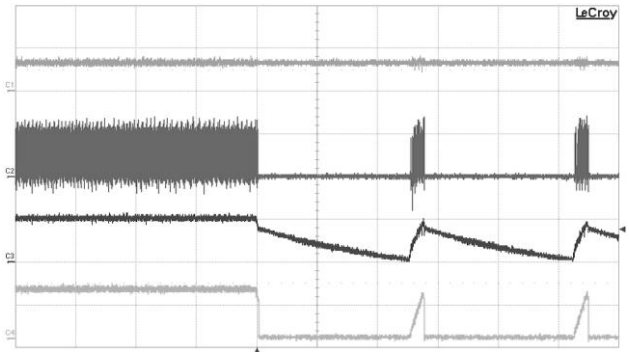


Shutdown 10 A Load 1 V_{DET}, 2 DL, 3 SS, 4 V_{OUT}

Figure 5. Shutdown Waveforms

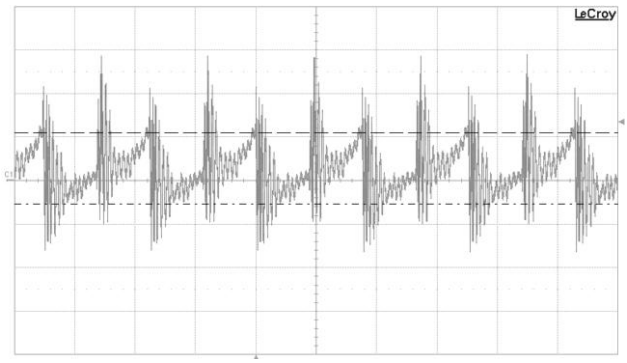


25 A Load 1 V_{DET}, 2 DL, 3 SS, 4 V_{OUT}

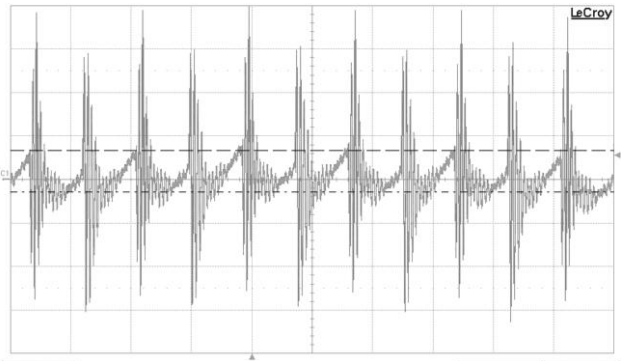


25 A Load 1 V_{REF}, 2 DL, 3 SS, 4 V_{OUT}

Figure 6. Over Current Protection/Hiccup Waveforms

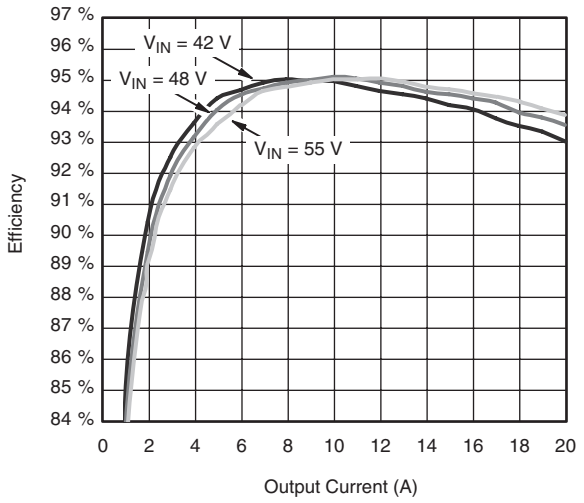


No Load 33 mV_{pk-pk}



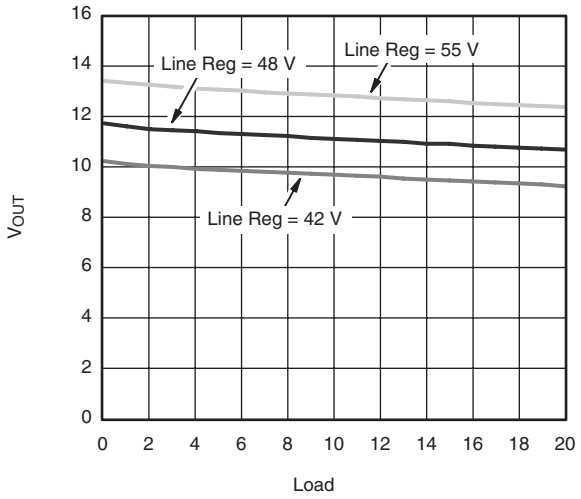
10 A Load 47 mV_{pk-pk}

Figure 7. Ripple Waveforms



SiP11206 1/16th Brick Efficiency

Figure 8. Efficiency



1/16th Brick Line-Load Regulation

Figure 9. Line-Load Regulation

PCB LAYOUT

The demo board is an 10 layer board in the sixteenth-brick form factor, manufactured with 2 oz copper on the outer layers and 3 oz copper on the inner layers. The circuit schematics for the demo board are illustrated in figures 10 and 11.

The transformer is a planar magnetic component with an EI core. The primary winding has 4 turns, located on layers 2, 4, 5 and 7, with 1 turns per layer. Each secondary winding has 2 turns, located on layers 1, 3, 6, and 8 with 2 turn per layer. The auxiliary winding has 2 turns, consisting of 2 turns on the bottom layer figure 12. Figure 13 shows the top bottom of the base board.

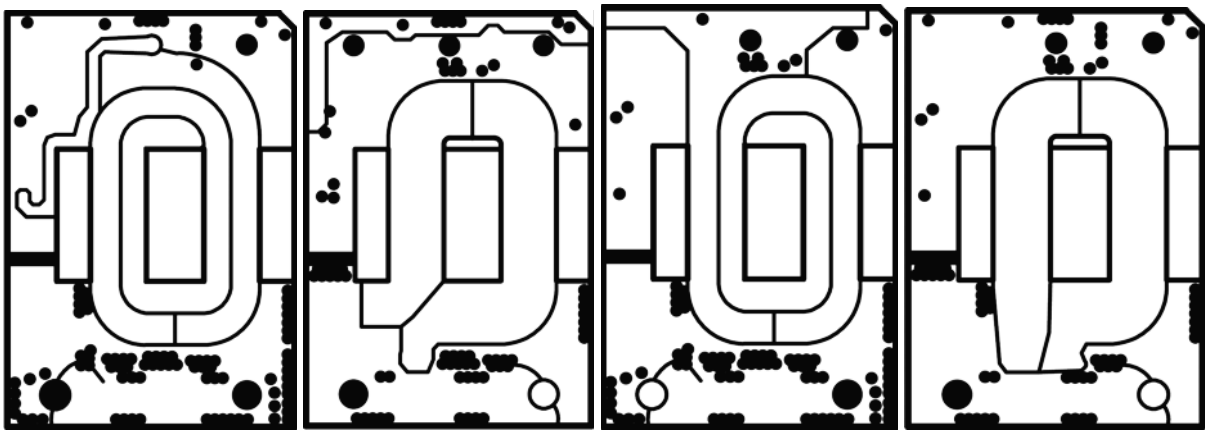


Figure 10. Layers 1 to 4 of PCB (l-r)

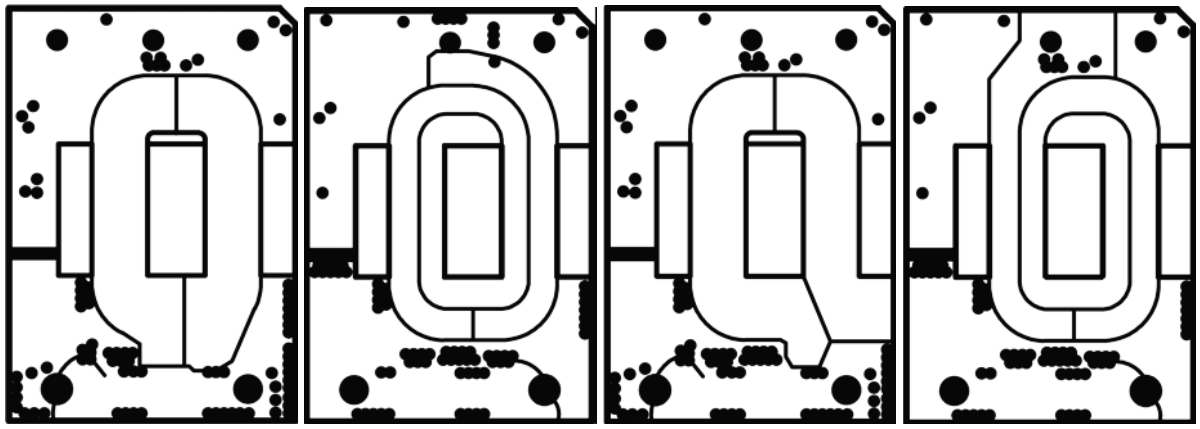


Figure 11. Layers 5 to 8 of PCB (l-r)

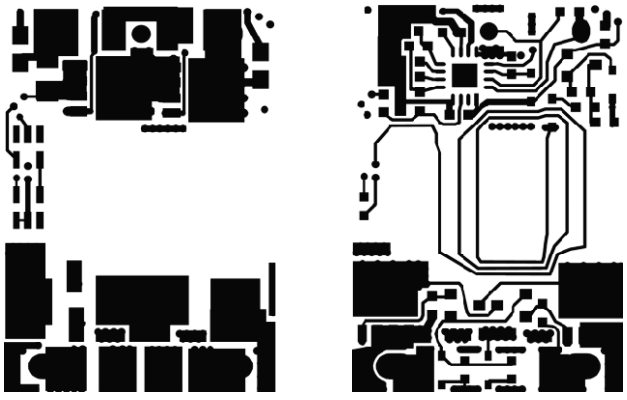


Figure 12. Top and Bottom Layout

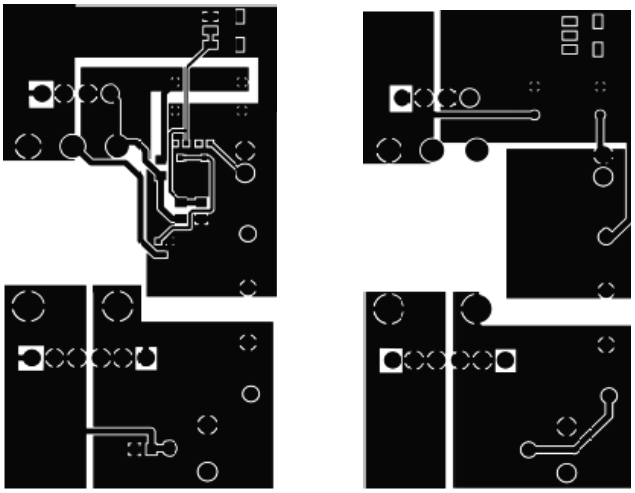


Figure 13. Top and Bottom PCB layout of Base Board

The schematics are shown in figures 14 and 15, and parts list are shown in table 1 and 2.

TABLE 1 - IBC PARTS LIST - PART VALUES ARE FOR NARROW INPUT VERSION

Designator	Description	Comment	Footprint	Quantity	Value
C1	Capacitor		603	1	100 nF/25 V
C3	Capacitor		603	1	1 µF/16 V
C4	Capacitor		402	1	100 pF/25 V
C5	Capacitor		402	1	22 nF/25 V
C6	Capacitor		402	1	220 pF/25 V
C8	Capacitor		1812	1	4.7 µF/50 V
C10	Capacitor		1812	1	4.7 µF/50 V
C12	Capacitor		603	1	0.1 µF/25 V
C13	Capacitor		603	1	1 µF/16 V
C14	Capacitor		1812	1	22 µF/16 V
C15	Capacitor		1812	1	22 µF/16 V
C17	Capacitor		603	1	0.1 µF/25 V
C18	Capacitor		603	1	1 µF/16 V
D1	Default Diode	BAV19WS	SOD323/X.85	1	
D5	Schottky Diode	SSC54	Diode SMC	1	
D7	Schottky Diode	BAS170WS	SOD323/X.85	1	
D8	Schottky Diode	BZX384B11-11V2 %	SOD323/X.85	1	
D9	Schottky Diode	BAS170WS	SOD323/X.85	1	
D10	Schottky Diode	BZX384B11-11V2 %	SOD323/X.85	1	
L1	Inductor	IHLP2525CZ-01	IHLP2525CZ-01	1	0.47 µH
P1		V_{IN}	Pin-through-hole	1	3102-3-00-xx-00-00-08-0
P2		On/Off	Pin-through-hole	1	3102-3-00-xx-00-00-08-0
P3		GND	Pin-through-hole	1	3102-3-00-xx-00-00-08-0
P4		12 V_O	Pin-through-hole	1	3144-3-00-xx-00-00-08-0
P5		0 V	Pin-through-hole	1	3144-3-00-xx-00-00-08-0
Q1	Synch MOSFET	Si7174DN	PowerPAK-1212-8-single	1	
Q2	Synch MOSFET	Si7174DN	PowerPAK-1212-8-single	1	
Q3	MOSFET	Si2308DS	SOT23	1	
Q4	Synch MOSFET	Si7156DN	PowerPAK-1212-8-single	1	
Q5	Synch MOSFET	Si7156DN	PowerPAK-1212-8-single	1	
Q7	SOT23 NPN Silicon	ZXTN2031F	SOT23	1	
Q8	MOSFET	Si2308DS	SOT23	1	
R1	Resistor		402	1	82K
R2	Resistor		402	1	80.6K
R3	Resistor		402	1	220R/1 %
R5	Resistor		402	1	33K/1 %
R6	Resistor		402	1	3.6K/1 %
R7	Resistor		402	1	10 R
R9	Resistor		402	1	100K
R10	Resistor		402	1	100K
R12	Resistor		402	1	82K
R15	Resistor		402	1	10K

TABLE 1 - IBC PARTS LIST - PART VALUES ARE FOR NARROW INPUT VERSION

Designator	Description	Comment	Footprint	Quantity	Value
R16	Resistor		402	1	10K
R17	Resistor		1206	1	0.01 R
R18	Resistor		402	1	1.5K/1 %
R19	Resistor		402	1	1.5K
T1		EI-18 Planar	E18-Planar-TFM	1	
U1	PWM CTLR	SiP11206	MLP44-16-Pitch 0.65 mm	1	
U2	Temperature Sensor	LM26-Thermal-Sensor	SO-G5/P.95	1	
Z1	Micropower Voltage Reference	LM4120-V_{REF}	SO-G5/P.95	1	

TABLE 2 - BASE BOARD PARTS LIST

Designator	Description	Comment	Footprint	Quantity	Value
COAX-F	Coax-F Connector	1	H3183-05	1	
COAX-F	Coax-F Connector	2	H3183-05	1	
COAX-F	Coax-F Connector	3	H3183-05	1	
Cap2	Capacitor	C1	RB5-10.5	1	47 µF/160 V
Cap2	Capacitor	C2	RB5-10.5	1	100 pF
Cap Semi	Capacitor (Semiconductor SIM Model)	C3	CR3216-1206	1	100 pF
BAS16	Silicon Switching Diode for High-Speed Switching	D1	SO-G3/C2.5	1	
BAS16	Silicon Switching Diode for High-Speed Switching	D2	SO-G3/C2.5	1	
Fuse 2	Fuse	F1	CR3216-1206	1	
COAX-F	Coaxial-Connection	J4		1	
Test Point	Test Point	J8	0364-0-15-01-13-27-10-0	1	
Test Point	Test Point	J9	0364-0-15-01-13-27-10-0	1	
Header 6	Header, 6-Pin	JP1	1727056	1	
Header 4	Header, 4-Pin	JP2	1727036	1	
MHDR1X2	Header, 2-Pin	JP3	1727010	1	
MMUN2213LT1G	NPN Bipolar Transistor	Q1	SO-G3/X.9	1	
Res1	Resistor	R2	CR3216-1206	1	16K
Res1	Resistor	R3	CR3216-1206	1	1.5K
SW-SPDT	SPDT Toggle Switch	S1	ET01MD1	1	
Test Point	Test Point	TP4	20-313137	1	
Test Point	Test Point	TP1	20-313137	1	
Test Point	Test Point	TP2	20-313137	1	
Test Point	Test Point	TP3	20-313137	1	

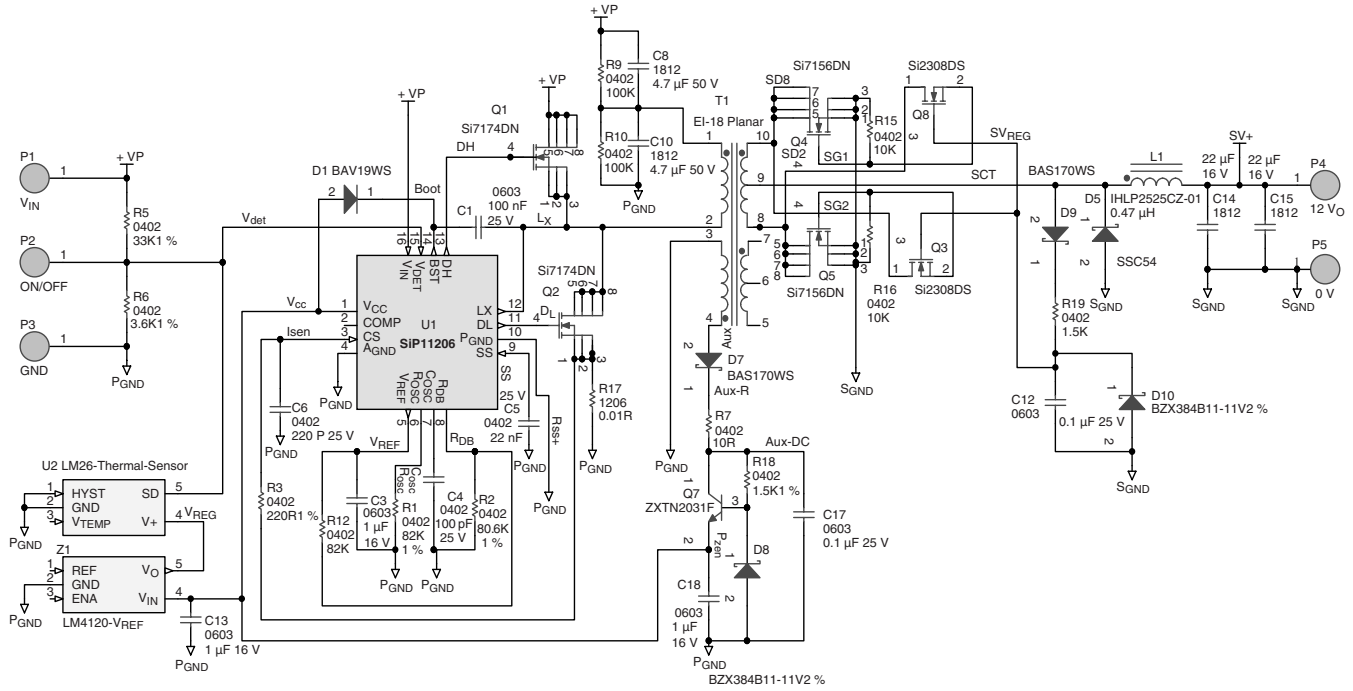


Figure 14. Schematic

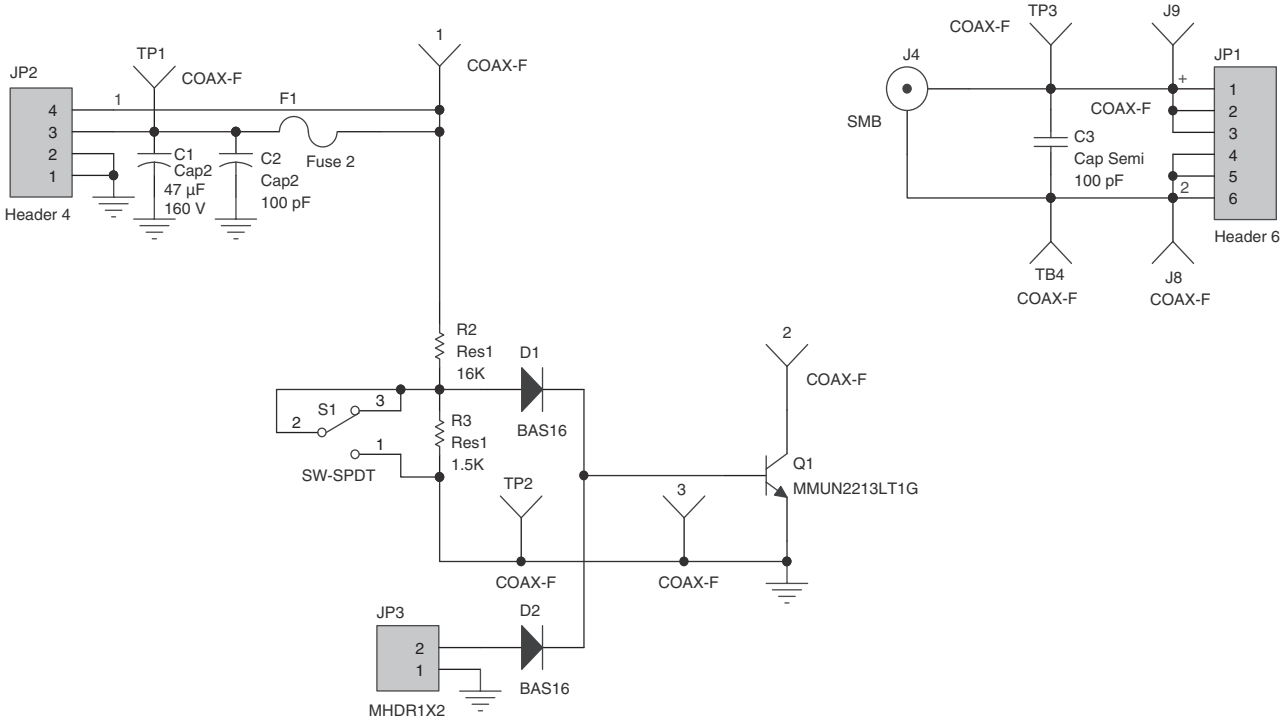


Figure 15. Schematic - Base Board

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